ABSTRACT

There are known high-speed devices for bringing the numbers modulo with a pre-determinant of the deductible module, which are built on the basis of three binary summators. Such devices are characterized by high hardware costs, especially in the construction of matrix and conveyor schemes. On the basis of one binary adder and three comparison schemes, a high-speed partial residue generator is proposed. This allows to simplify the hardware cost to bring the different bit numbers on the module for pre-determining the deductible of the module. The proposed shaper partial balances checked by running on the platform Artix-7 from the company Xilinx with Verilog language prektirovaniya.